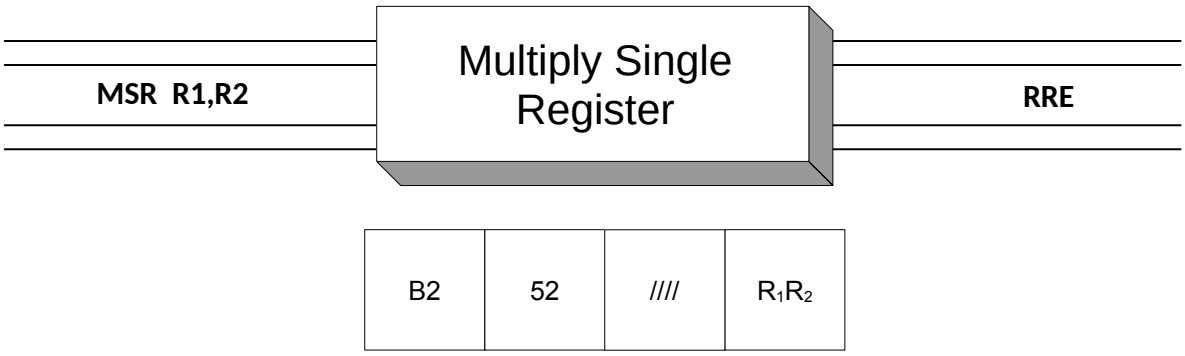
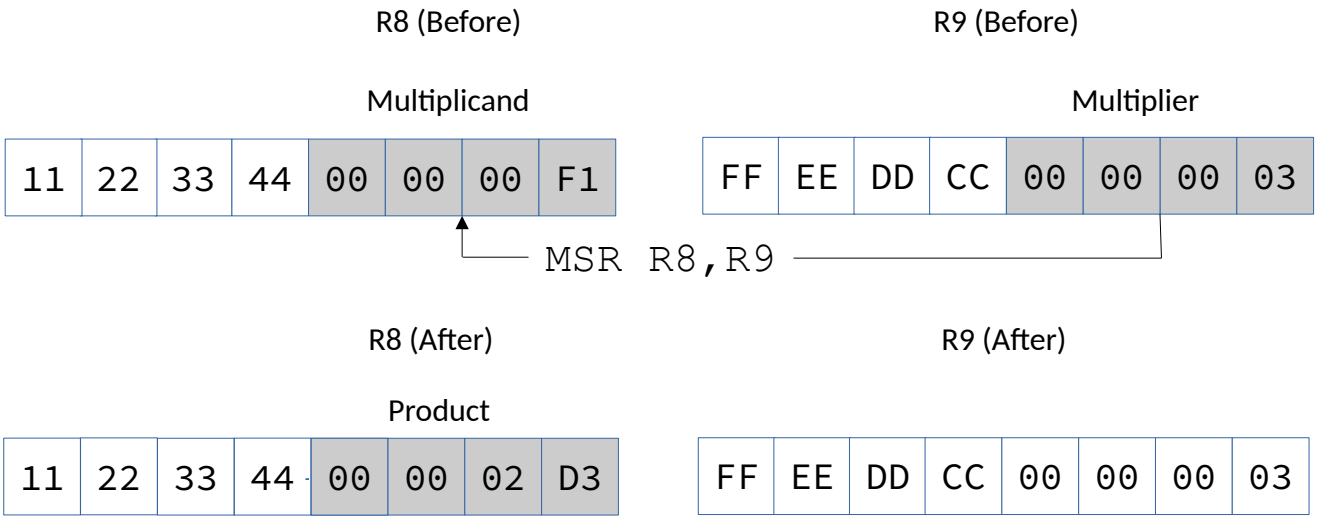


Multiply Single Register (**MSR**) produces a 32-bit signed binary product in bits 32-63 of R_1. Before multiplying, the multiplicand is in bits 32-63 of R_1 and the multiplier is in bits 32-63 of R_2. Both the multiplicand and the multiplier are 32-bit signed binary integers. After multiplication, the rightmost 32 bits of the product are placed in the rightmost 32 bits of R1. The leftmost 32 bits of R1 remain unchanged. The leftmost 32 bits of R1 are not tested for significance. As a result, the condition code is unchanged, and overflows are not detected.

Consider the following example,



Examples

Some Unrelated Multiply Single Registers (MSRs)

```
R4 =  X'12121212_00000002'          UNDERSCORE _ FOR READABILITY
R5 =  X'00000000_00000003
R6 =  X'00000000_0000000F'
R7 =  X'00000000_7FFFFFFF'          LARGEST POSITIVE MULTIPLIER
R8 =  X'00000000_FFFFFFFF'          MULTIPLIER = -1

                                AFTER MSR         UNDERSCORE _ FOR READABILITY
      MSG   R4,R5               R4 = X'12121212_00000006'   2 x 3 = 6
                                R5 = X'00000000_00000003'

      MSG   R4,R6               R4 = X'12121212_0000001E'   2 x 15 = 30
                                R6 = X'00000000_0000000F'

      MSG   R4,R7               R4 = X'12121212_FFFFFFFE'   2 x 2,147,483,647 = -2
                                R7 = X'00000000_7FFFFFFF'   OVERFLOW NOT DETECTED

      MSG   R4,R8               R4 = X'12121212_FFFFFFFE'   2 x -1 = -2
                                R8 = X'00000000_FFFFFFFF'
```

Tips

1) Use this instruction to easily multiply 32-bit values in registers that produce single-precision results.

2) This instruction produces a 32-bit product. The generated result must be in the range +2,147,483,647 and -2,147,483,648.

3) The condition code is not set by this instruction, so overflows will not be detected.