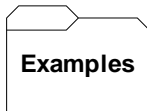


The And Register instruction performs a logical bit by bit “and” between two registers. Operand 1, the target, is a register and Operand 2, the source, also specifies a register. The fullword in Operand 1 is “and-ed” internally with the fullword in Operand 2, and the result is placed in Operand 1. The table below shows the results of “and-ing” two bits together.

Bit 1	Bit 2	Bit 1 and Bit 2
0	0	0
0	1	0
1	0	0
1	1	1

This instruction sets the condition code as follows:

- 0 if all target bits are set to 0. Test this condition with **BZ** or **BNZ**.
- 1 if any target bit is set to 1. Test this condition with **BM** or **BNM**.



Some Unrelated And Registers

```
R4 = X'FFFFFFFF'    ALL 1'S
R5 = X'00000000'    ALL 0'S
R6 = X'0000148C'    000000000000000000001010010001100
R7 = X'000014AB'    000000000000000000001010010101011
```

```
NR  R4,R4    R4 = X'FFFFFFFF' Condition Code = 1
NR  R4,R5    R4 = X'00000000' Condition Code = 0
NR  R4,R6    R4 = X'0000148C' Condition Code = 1
NR  R4,R7    R4 = X'000014AB' Condition Code = 1
NR  R5,R6    R5 = X'00000000' Condition Code = 0
NR  R5,R7    R5 = X'00000000' Condition Code = 0
NR  R6,R7    R6 = X'00001488' Condition Code = 1
NR  R7,R7    R7 = X'000014AB' Condition Code = 1
```