Load Register

LR   R1,R2   RR

Op Code	R₁R₂

The Load Register instruction copies the rightmost 32 bits of the register specified by Operand 2, into the rightmost 32 bits of the register specified by Operand 1. The contents of Operand 2 are unchanged as well as the condition code. Consider the instruction below.
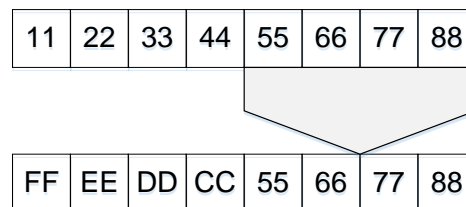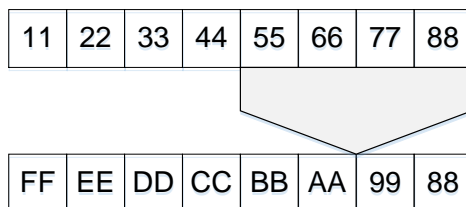
```
LR    R9,R8
```

The rightmost 32 bits (4 bytes) of register 8 are copied to rightmost 32 bits of register 9, destroying the previous value in register 9.   The high-order 32 bits of register 9 are unchanged. The contents of register 8 are unaffected by the operation. The diagram below illustrates this operation.
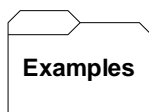
```
LR      R9,R8
```

R8 (Before)   R8 (After)

| 11 | 22 | 33 | 44 | 55 | 66 | 77 | 88 | | 11 | 22 | 33 | 44 | 55 | 66 | 77 | 88 |

| FF | EE | DD | CC | BB | AA | 99 | 88 | | FF | EE | DD | CC | 55 | 66 | 77 | 88 |

R9 (Before)   R9 (After)

Examples

Some Unrelated LR's

```
R4  =   X'FFFFFFFF'
R5  =   X'00000028'
R6  =   X'00000004'

LR     R4,R5      R4 = X'00000028'  R5 = X'00000028'
LR     R5,R4      R5 = X'FFFFFFFF'  R4 = X'FFFFFFFF'
LR     R5,R6      R5 = X'00000004'  R6 = X'00000004'
LR     R6,R5      R6 = X'00000028'  R5 = X'00000028'
```